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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,864	02/21/2002	Masahiro Yonemochi	39-02	7562

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PAUL AND PAUL
2900 TWO THOUSAND MARKET STREET
PHILADELPHIA, PA 19103

EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,864	YONEMOCHI, MASAHIRO	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *21-23* is/are withdrawn from consideration.

5)☒ Claim(s) *14-20* is/are allowed.

6)☒ Claim(s) *1-6 and 11-13* is/are rejected.

7)☒ Claim(s) *7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of group I invention, claims 1-20 in Paper filed November 21, 2003 is acknowledged. The traversal is on the ground(s) that the interest of overall efficiency on the part of the Applicant. This is not found persuasive because Applicant failed to prove a lack of distinction between the two independent inventions.

2. The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs, U.S. Patent 5,482,898 in view of Huang et al., U.S. Patent 6,400014 B1.

Marrs discloses a semiconductor device substantially as claimed. See **FIGS. 1-8** where Marrs substantially teaches the claimed invention.

5. Pertaining to claim 1, Marrs discloses a heat spreader adapted **108** to be insert-molded with resin on a surface of a circuit board on which a semiconductor chip is mounted so that said heat spreader covers said surface of the circuit board including an upper surface of said semiconductor chip **106** over substantially a same area as that covered with molded resin **110** when insert-molded with resin, said heat spreader having:

a first (top), main portion which defines a first gap (i.e., distance between the heat spreader **108a** and the top of the semiconductor chip **106**) with respect to said surface of the circuit board when insert-molded with resin; and

a second portion which defines a second gap **108b** with respect to said surface of the circuit board when insert-molded with resin, said second gap being smaller than said first gap, so that at least said second portion is embedded in said mold resin when insert-molded with resin.

However, Marrs fails to disclose that encapsulant **110** is a resin. Huang teaches that encapsulant can be a resin. In view of Huang, it would have been obvious to one of ordinary skill in the art to incorporate the resin body of Huang into the Marrs semiconductor device because a BGA package is typically encapsulated by the resin body (column 1, lines 20-23).

6. Pertaining to claim 2, Marrs fails to teach a heat spreader as set forth in claim 1 further comprising a plurality of third portions which are in contact with said surface of the circuit board when insert-molded with resin. Huang teaches a plurality of third portions which are in contact with said surface of the circuit board when insert-molded with resin. See **FIG.1** of Huang where a third portion of a heat spreader is in contact with circuit board **30**. In view of Huang, it would have been obvious to one of ordinary skill in the art to incorporate the features of Huang into the Marrs semiconductor device because it provides support for the planar plate (column 4, lines 13-15).

7. Pertaining to claim 3, Marrs in view of Huang discloses a heat spreader as set forth in claim 2, wherein said third portions are provided on said second portions.

8. Pertaining to claim 4, Marrs teaches a heat spreader **108** adapted to be insert-molded with resin on a surface of a circuit board on which a semiconductor chip is mounted so that said heat spreader covers said surface of the circuit board including an upper surface of said semiconductor chip over substantially a same area as that covered with molded resin when insert-molded with resin, said heat spreader comprising:

a first surface positioned at a side of said circuit board and adhered with resin when insert molded with resin; and

a second surface positioned opposite to said first surface and at least a part thereof defining an exposed surface when insert-molded with resin;

said heat spreader further comprising:

a first part, at the first surface thereof, defining a first gap with respect to said surface of the circuit board when insert-molded with resin and, at the second surface thereof, defining said exposed surface when insert-molded with resin; and

a second part, at the first surface thereof, defining a second gap with respect to said surface of the circuit board when insert-molded with resin, said second gap being smaller than said first gap and, at the second surface thereof, being adhered to and embedded in resin when insert-molded with resin. However, Marrs fails to disclose that encapsulant **110** is a resin. Huang teaches that encapsulant can be a resin. In view of Huang, it would have been obvious to one of ordinary skill in the art to incorporate the resin body of Huang into the Marrs semiconductor device because a BGA package is typically encapsulated by the resin body (column 1, lines 20-23).

9. Pertaining to claim 5, Marrs fails to disclose a heat spreader as set forth in claim 4 further comprising a plurality of third parts, at the first surface thereof, which are in contact with said surface of the circuit board when insert-molded with resin. Huang teaches a plurality of third portions which are in contact with said surface of the circuit board when insert-molded with resin. See **FIG.1** of Huang where a third portion of a heat spreader is in contact with circuit board **30**. In view of Huang, it would have been obvious to one of ordinary skill in the art to incorporate the features of Huang into the Marrs semiconductor device because it provides support for the planar plate (column 4, lines 13-15).

10. Pertaining to claim 6, Marrs in view of Huang discloses a heat spreader as set forth in claim 4, wherein said third parts are provided on said second
part.

11. Pertaining to claim 11, Marrs discloses a semiconductor device comprising:
a circuit board having a surface**113**;
a semiconductor chip **106** mounted on said surface of the circuit board; and
a heat spreader **108** having a first, main portion which defines a first gap to said surface of the circuit board, and a second portion which defines a second gap to said surface of the circuit board, said second gap being smaller than said first gap; and
a resin insert-molded with said heat spreader integrally on said surface of the circuit board

so as to cover an area of said surface including an upper surface of said semiconductor chip, so that at least said second portion is embedded in said resin. However, Marrs fails to disclose that encapsulant **110** is a resin. Huang teaches that encapsulant can be a resin. In view of Huang, it would have been obvious to one of ordinary skill in the art to incorporate the resin body of Huang into the Marrs semiconductor device because a BGA package is typically encapsulated by the resin body (column 1, lines 20-23).

12. Pertaining to claim 12, Marrs in view of Huang teaches a semiconductor device as set forth in claim 11, wherein said heat spreader further comprises a plurality of third portions which are in contact with said surface of the circuit board. Huang teaches a plurality of third portions which are in contact with said surface of the circuit board when insert-molded with resin. See **FIG.1** of Huang where a third portion of a heat spreader is in contact with circuit board **30**. In view of Huang, it would have been obvious to one of ordinary skill in the art to incorporate the features of Huang into the Marrs semiconductor device because it provides support for the planar plate (column 4, lines 13-15).

13. Pertaining to claim 13, Marrs in view of Huang discloses a semiconductor device as set forth in claim 12, wherein said third portions are provided on said second portions.

Drawings

14. The drawings are objected to under 37 CFR 1.83(a) because they fail to show element 3 and element 4 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Objection

15. Claims 7, 8, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

16. Claims 14-20 allowed.

17. The following is an examiner's statement of reasons for allowance: the combination of the prior art does not disclose a heat spreader which is recessed near the semiconductor chip and attached to the circuit board in which the semiconductor chip is attached.

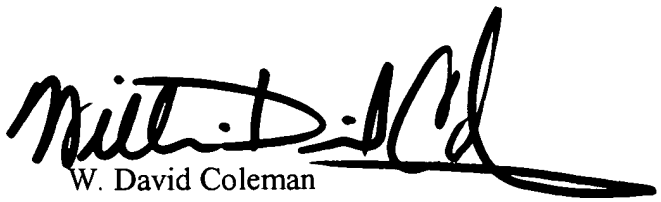
18. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman
Primary Examiner
Art Unit 2823

WDC